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Computer-Aided Design AND APPLICATIONS

Design Optimization of Complex Products Based on CAD Multi-Objective Genetic Algorithm

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Abstract. To solve the continuous development of integrated circuits makes the design more and more complex and due to the IC market competition. CAD offers sophisticated product design optimizations based on multi-purpose genetic algorithms. An improved method for calculating the Pareto-optimal solution of a CMOS analog circuit based on a non-dominant classification genetic algorithm (NSGA-II). Check the feasibility of the method, the equation-based, simulation-based optimization and improved methods are compared respectively, it is obvious to see the advantages and disadvantages of the first two methods, namely the equation-based optimization is very fast, but the accuracy is low, while the simulation-based optimization has high accuracy, but is slow and takes a lot of time, and the improved method has clearly formed a Pareto optimal curve when it evolved to the 80th generation. The proposed model is improved the evolutionary efficiency by 40 generations over simulation-based optimized design, equivalent to a time reduction of approximately 8 hours. It only takes about 12 hours to reach the optimization, and the error rate is only 10%.

Keywords: Analog circuit optimization; Multi-objective genetic algorithm; Pareto optimal frontier; CAD.
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1 INTRODUCTION

The engineering optimization design can make the designed product structure the most reasonable, the best performance, the highest quality and the lowest cost within the allowable range [1]. CAD systems may perform a range of scans and tests to ensure that the product can

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sustain the reported weight and withstand the desired pressure [2, 3]. Good design may also benefit the production process. If your manufacturer reports fewer draught products and wastes, your things will be cheaper and faster in the end. Faulty design may become a thing of the past with a strong CAD system [4, 5]. One advantage of using CAD software is that it automatically generates documentation. When you have documentation, you have reasons for system design as well as simple explanations to keep people from asking stupid questions [6, 7].

CAD technology can reduce repetitive labor, shorten design cycle and improve design quality. How to seamlessly integrate the optimization method and the CAD modeling process is an urgent problem to be solved, the author conducts preliminary research and exploration with circuit optimization design as an example [8]. CAD provides benefits over manual designs that have made it an unavoidable need in today's design business. These innovative approaches benefit the modern engineer or product designer in a variety of ways. Saving time directly leads into increased output. The same amount of time might result in a greater number of jobs accomplished. The correctness of D design is unsurpassed, with nearly no mistakes. This provides it with a significant edge over manual designing and drawing. With the rapid development of microelectronic technology and VLSI design technology, integrated circuits have entered the Nano era, 90nm, 45nm and 32nm CMOS processes have been widely used, and the chip wafer has also reached 300mm, now the 22nm process has been successfully developed and will be mass-produced soon. Very-large-scale integration refers to the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip (VLSI). Since the development of very large-scale integration (VLSI) designs, the number of applicants of integrated circuits (ICs) in increased computing, controls, telecommunications, computer vision, and consumer electronics has been quickly rising.

The acronym for "Complementary Metal Oxide Semiconductor" is "Complementary Metal Oxide Semiconductor." This is one of the most extensively used technologies in the computer chip design industry, with integrated circuits used in a variety of applications. From a vertical perspective, driven by the continuous introduction of new technologies, the improvement of IC chip integration and the reduction of process feature size continue to maintain Moore's Law. Moore's law predicts that every two years, the number of transistors packed onto a computer chip will double. Exotic materials, new packaging technologies, and more complex 3D designs will all be included in next-generation chip designs. The semiconductor industry will bring together engineers from a wide spectrum of physical, chemical, biological, and computer sciences to realize these breakthrough innovations. From a horizontal perspective, integrated circuits are constantly changing the traditional industrial division of labor by combining other disciplines and specialties to form new directions or technologies.

In the past decade or so, an important development trend is the emergence of a more and more complex System on Chip (SOC, System on Chip). A SoC is an IC that combines all of the components into a single chip. It may include analogue, digital, mixed signal, and other radio frequency functions on a single chip substrate. It consumes less electricity and is reasonably priced. It also has a high degree of reliability. SoCs are currently widely employed in the electronics industry because to their low power consumption. SoCs are also widely used in embedded system applications. At present, SOC technology platforms for various application fields have appeared. Such as the fourth-generation mobile communication SOC platform, information security SOC platform, high-definition video multimedia SOC platform and home network SOC platform [9, 10]. As the name indicates, a SoC is a complete processing system in a single package. It is not a single processor chip package, as you may be aware if you have ever built a computer [11, 12]. An SoC, on the other hand, integrates many processing elements, memory, communications, and other crucial bits and pieces onto a single chip that is installed on a circuit board. By integrating numerous components into a single chip, space, cost, and power consumption are all decreased [13, 14]. An SoC is your smartphone's brain, managing everything from the Android operating system to detecting when the power button is touched. SoCs are linked to cameras, displays, RAM, flash storage, and other components [15, 16].

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Moreover, simulation optimization software assists designers in lowering manufacturing costs, working quicker and smarter, and completing projects more quickly. This allows businesses to produce high-quality; low-cost goods while also allowing them to distribute products more rapidly and make changes on the fly as needed. This represents a huge competitive advantage in the global economy. Software may be used to build, modify, and optimize the design process. CAD may be used to create, modify, and optimize the design process. Automation, data visualization, artificial intelligence (AI), vertical reality (VR), and artificial reality (AR) will all be significant advancements in the sector. Among the uses of the design program are complete dentures and removable partial denture frameworks. The hive is capable of learning in ways that humans are not. The development of SOC brings the biggest challenge to the designer, is to put forward the design requirements of integrating digital circuits and analog circuits into one chip at the same time, which is a highly complex and difficult task.

In order to shorten the design time and reduce the design cost, it is necessary to rely on effective design automation (EDA) tools. Currently for digital integrated circuits, there are relatively complete automatic design and synthesis technologies, and there are quite mature EDA tools from high-level circuit synthesis to low-level layout. The designer's design ideas can be converted into circuit topology and physical layout in a short time [17]. EDA, also known as electronic computer-aided design (ECAD), is a set of software tools used to develop electronic systems such as integrated circuits and printed circuit boards. The tools are used by chip designers as part of a design pipeline to construct and test entire semiconductor devices [18, 19]. EDA tools are critical for the design of modern microelectronic devices, which include billions of elements; this article focuses on EDA for integrated circuits in particular (ICs) [20, 21].

Figure 1 is a complete design process based on VHDL hardware description language, which is mainly composed of modules such as design and entry, design synthesis, functional simulation, design implementation, layout and routing, and timing simulation. The model in the figure 1 illustrates the SOC design process. It puts forward the design requirements of integrating digital circuits and analog circuits into one chip at the same time. With this platform design cycle will be shorten and have improved design quality.

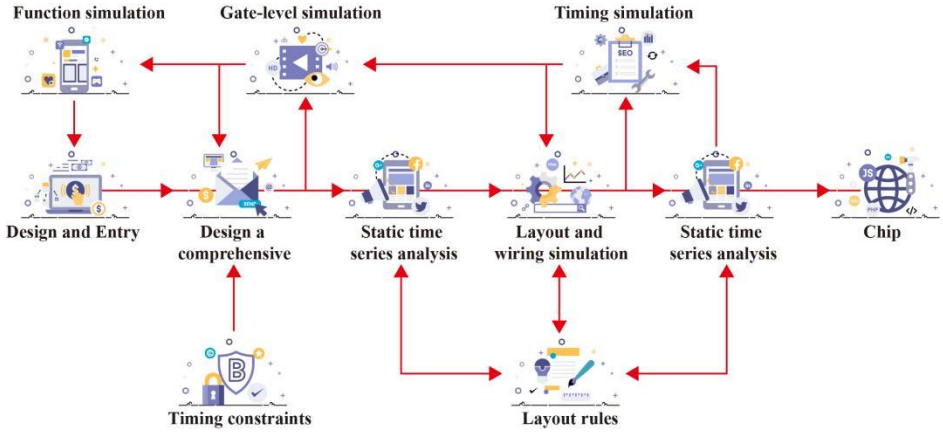

Figure 1: A complete SOC design process.

The opposite of this is the design of analog integrated circuits. Due to various reasons, the research on design automation technology of analog integrated circuits is far behind that of digital integrated circuits. At present, most of the analog integrated circuit designs still use the traditional manual design method, that is, circuit design experts, on the basis of past experience and intuition, a simplified circuit model is used for a preliminary design, and then it is repeatedly simulated and modified using a circuit simulator until a predetermined performance requirement is achieved. The

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consequence of this is that in SOC design, although most of the circuits are digital in proportion, and analog circuits only account for a small part, the design time and cost of analog circuits are often more than those of digital parts due to the difficulty of designing analog circuits [22]. This situation obviously cannot meet the design needs of more and more SOCs in the future. The crux of the problem is to improve the automation level of analog integrated circuit design, so as to shorten the design time and reduce the design cost.

2 LITERATURE REVIEW

Due to the diversification of the types and structures of analog integrated circuits, the circuit performance indicators are numerous and mutually restrictive, and the optimal design of analog integrated circuits is quite complicated. Taking the operational amplifier as an example, the octagonal rule for the design of analog amplifiers has many circuit structures, such as Cascade, Folded, Telescope and Differential. And so on, its performance indicators are also many, including slew rate (Slew-Rate), unity gain bandwidth (Unity Gain Bandwidth), DC gain (Gain), power consumption (Power consumption), phase margin (Phase Margin), input and output impedance (Rin Rout), settling time (set-time), power supply voltage rejection ratio (PSRR), noise (Noise), there are dozens of items such as offset voltage and harmonic distortion, and it is usually difficult to give a single and complete design goal [23]. At the same time, most of these performance parameters will restrict each other.

There is generally no single circuit that is optimal for all metrics over all ranges. Such mutual constraints and compromises present many difficulties in the optimal design of analog circuits. Basically, analog integrated circuit design is a multi-purpose optimization problem [24]. Analog integrated circuit design is a creative process. Contrary to the process of circuit analysis, which uses the circuit as the starting point to discover its characteristics, it mainly uses the circuit to achieve the design goal, start with a set of desired performance parameters to find a satisfactory circuit. Analog integrated circuit design is considered a broad-based, multi-stage, re-ranking task. It often takes a long time, and the entire design process needs to use a lot of technology [25, 26]. The method used in the vast majority of analog integrated circuit designs at present; it is still a bottom-up design method, and its design process see Figure 2.

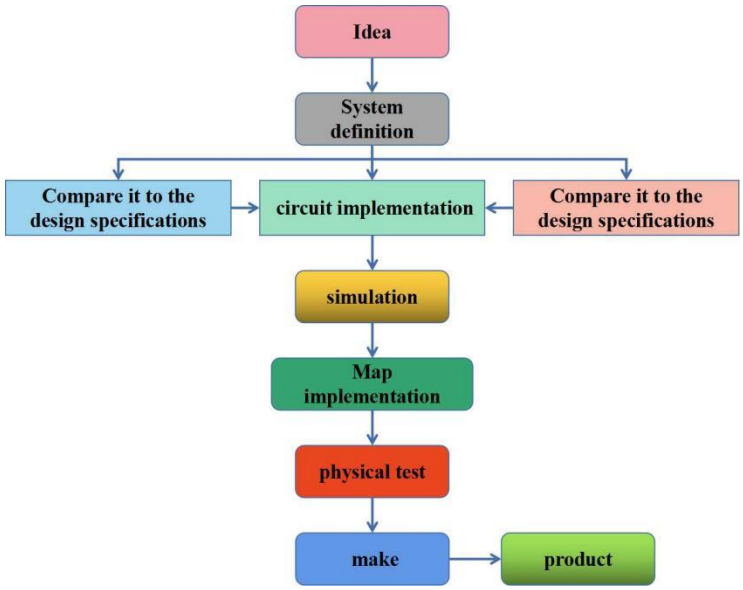

Figure 2: Design process of an analog integrated circuit.

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Throughout the process, the designer is responsible for all stages except the manufacturing stage. First of all, the circuit designer conceives according to the needs of the problem, defines various design requirements, and selects the circuit structure according to experience. Then use circuit simulators (such as SPICE, Hspice, Spectre, etc.) to repeatedly synthesize and simulate the simulation circuit, including the simulation of power consumption, current, voltage, temperature, slew rate, input and output, gain, frequency and other parameters, continuously adjust and improve the circuit according to the obtained simulation results until it meets the requirements. Then proceed to another major work - layout design. The circuit layout involves the geometric and physical description of the silicon wafer circuit.

After the layout is completed, it must be repeatedly physically verified (such as device matching, symmetry, interference and other constraints must be taken into account) [27]. At the same time, the layout is continuously improved until it is successful, and finally the parasitic effects generated by the layout and routing are taken into account and the simulation is carried out again, if parasitic effects affect the circuit, the layout needs to be adjusted, if the layout still cannot be solved, the circuit may have to be improved, so that it is repeated, the various stages until the final result meets the design requirements, and the product can be manufactured. The chips produced at this time have to be thoroughly tested. If the test is successful, it can be put into mass production. If the test fails, it needs to be returned to allow the designer to make further adjustments to the layout or the circuit itself [28].

After selecting the circuit structure in the front-end design, the parameter determination (ie Sizing) can be regarded as an optimization problem. As mentioned earlier, this is essentially a multi-objective optimization problem, i.e., two or more competing objectives need to be coordinated and weighed. In the past, the traditional way to solve this problem was to combine all the objectives into one evaluation function. In general, this merit function is obtained by linearly weighing all objective functions and punitive functions. An optimal solution can be obtained by solving this global evaluation function [29]. However, because the goals are conflicting, it is difficult to create a truly optimal one-objective function. There are no objective criteria for weight selection, and different optimization results will be obtained when selecting weights. These shortcomings hinder the practical application of traditional circuit optimization methods [30]. Nonetheless, complex circuits are difficult to design and need specialized techniques. Debugging a malfunctioning VLSI device, for example, is difficult and time-consuming, as design modifications might take several weeks to several months. Long design cycles may result in missed opportunities to market the semiconductor and repay investment [31, 32].

3 RESEARCH METHODS

3.1 Optimization-Based Design Methods for Analog Integrated Circuits

Optimization-based device sizing is the replacement of circuit empirical formulas by optimization algorithms, that is, under the constraints of satisfying certain constraints, according to a certain mathematical optimization algorithm, the parameters of the components in the circuit are continuously adjusted until the target parameters meet the optimization requirements. This model can be basically divided into two models: model-based model (Simulation-based device size) and Equation-based model (Equation-based device size).

3.1.1 Simulation-based optimization design

The solution based on simulation optimization is to synthesize the optimization design problem of the analog circuit, and the circuit performance is calculated by using the SPICE circuit simulation simulator and high-precision device models (EKV, Philips MOS level 9, BSIM3, etc.). The process is shown in Figure 3.

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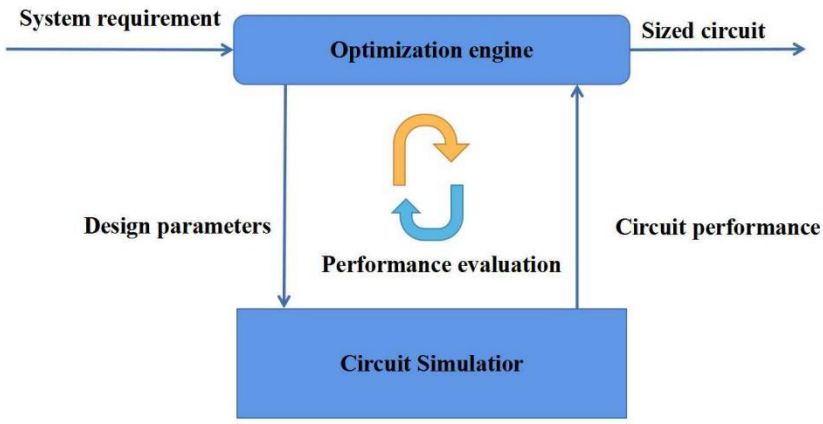

Figure 3: Simulation-based device sizing.

The optimization design process based on simulation is as follows:

1) Select a specific circuit according to the given performance requirements, process conditions and working environment.
2) Find the design variable which includes the value of the electric (R) capacitor (C) according to the selected circuit, geometry of transistors, and diodes.
3) The circuit is simulated by SPICE, and the corresponding electrical performance parameters are extracted from the simulation results.
4) The number of constraints is established based on the electrical structure. Under the specific working environment and performance requirements, the performance indicators of some circuits need to meet certain constraints.
5) The last step is to establish the objective function of circuit performance.

Using SPICE to simulate the circuit, in order to determine the performance index parameters that meet the requirements of the circuit, and to optimize the design goal is an iterative process. A complete circuit optimization is automatically carried out by the optimization program, which mainly includes: A limited number of circuit simulation iterations, continuous adjustment of the parameters of the components in the optimization process, repeated calls of the SPICE program in the iterative process, and evaluation and judgment of the simulation results [33].

The advantage of the design method based on simulation optimization is that it can handle a variety of circuit structures, and the high accuracy of the results can be guaranteed under the use of high-precision device models, the disadvantage is that the result of SPICE-like circuit simulator simulation can only be in the form of graph curves or tabular data, the data results thus provided contain a small amount of information, and it is too superficial, it is almost impossible to deduce the rain number expression of circuit performance, so it is difficult to understand the influence of various circuit parameters on circuit performance. Designers can only understand the relationship between circuit parameters and circuit performance through repeated simulations. At the same time, although the single simulation running time of the circuit simulator is very short (without considering the transient simulation), due to the need for thousands of repeated iterations to complete an automatic synthesis, as a result, the calculation amount of the entire design is huge and the calculation time is long, which usually takes several hours to dozens of hours.

3.1.2 Equation-based optimization design

Equation-based optimization design is the use of artificially derived equations for circuit performance, it can replace the circuit simulator to calculate the performance parameters of the circuit, which can overcome the defects of huge calculation amount and long calculation time based on simulation optimization, some analog integrated circuit automation design systems have

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adopted this method, such as OPASYN, STAIC, Maulik, FPAD (Fuzzy nonlinear Program for Analog circuit Design), AMGIE, ASTRX/OBLX, GPCAD (Geometrical programming CAD) and SD-OPT0, etc. The process is shown in Figure 4[33].

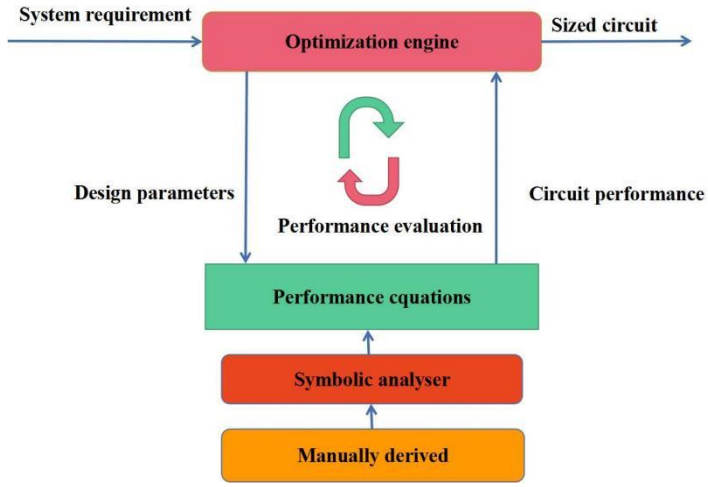

Figure 4: Equation-based device sizing.

3.2 Multi-Objective Evolutionary Algorithm

There is no single optimal solution to the problem of multi-target optimization in the world, and it is not possible to apply too many imperfect solutions directly. Therefore, domestic and foreign experts and scientists offer a variety of algorithms to solve the problem of multi-target optimization, of which many objective evolutionary algorithms (MOEAs) are the oldest and most widely used. The Multi-objective Evolution Algorithm (MOEA) is a type of global probability optimization search created by modeling biological evolution. A multi-objective evolution algorithm basically goes through two stages:

1) The algorithm of the first stage is mainly divided into the non-Pareto optimization method and the Pareto optimization method, wherein the non-Pareto method is highly efficient and easy to implement, but cannot generate some parts of the Pareto optimal front section; The Pareto optimization method uses non-inferior sorting to make the entire population approach the Pareto optimal front end.
2) The second stage is to combine external archives or external populations on this basis. By using external archives to store all non-dominated individuals of the current generation, the solution set can maintain a good degree of distribution, and at the same time, the elite retention strategy is adopted to make The algorithm search efficiency is significantly improved.

Multi-objective evolutionary algorithms have entered a period of comprehensive development, and various new concepts, mechanisms and strategies (such as hybrid strategies, parallel strategies, co-evolutionary strategies, quantum evolution strategies and dynamic evolution strategies, etc.) have begun to be introduced into MOEA, in order to obtain higher performance and more efficient algorithms, at the same time, the research of high-dimensional multi-objective optimization problem (MOOP) and dynamic multi-objective optimization problem (DMOP) has also made preliminary progress. Typical multi-objective evolutionary algorithms include non-dominated sorting genetic algorithm with elite strategy (NSGA-II), Pareto envelope selection algorithm (PESA2), intensity Pareto evolutionary algorithm (SPEA2), vector evaluation genetic algorithm (VEGA), multi-objective Genetic Algorithm (MOGA) and Niche Pareto Genetic Algorithm (NPGA), etc. The non-inferior solution individuals in the external concentration are output as the optimal

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solution, as shown in Figure 5. At present, MOEA has made great progress and certain achievements in many fields (such as engineering, industrial and scientific fields).

The optimal design based on circuit equations is equivalent to using simplified SPICE to simulate the simulation circuit that is, using simplified device model and circuit model, derive equations that describe circuit performance and circuit constraints, and then iteratively iterate these equations to calculate circuit performance. Therefore, this method does not need to call a large number of external programs and perform data access operations, making it much faster than the simulation-based optimization design, that is, the design time spent is far less than the simulation-based method, generally, it only takes a few seconds to tens of seconds.

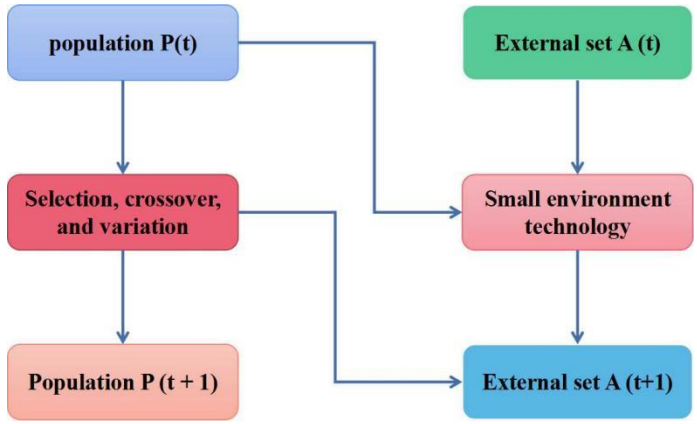

Figure 5: The general flow of the MOEA algorithm.

4 ANALYSIS OF RESULTS

4.1 Circuit Optimization Example

Figure 6 shows a basic two-stage un-buffered CMOS operational amplifier, which consists of V→I and I→V cascades, the first stage consists of M1, M2 to form a source-coupled differential pair, which converts the differential mode input voltage into differential mode current, this differential mode current acts on the current mirror loads M3 and M4 to restore the differential mode voltage. The second stage also means that the output stage is an active load common source amplifier stage composed of M6 and M7, which converts the input circuit of the second stage into a current, at the same time, the current is converted into a voltage at the output end of the load M7, which is acted on by this current. M8 and the current source I_{bias} form a bias circuit, which is used to determine the static operating point of the circuit. M5, M7 and M8 form a proportional constant current source, Cc is the Miller compensation capacitor, and CL is the load capacitor. The figure 6 is the circuit diagram for two stage CMOS op amp. A two-stage operational amplifier has a differential amplifier at the input stage, and the second stage is a high gain stage biased by the differential amplifier's output. The CMOS operational amplifier is the most complex and significant building component in linear CMOS and switched-capacitor circuits.

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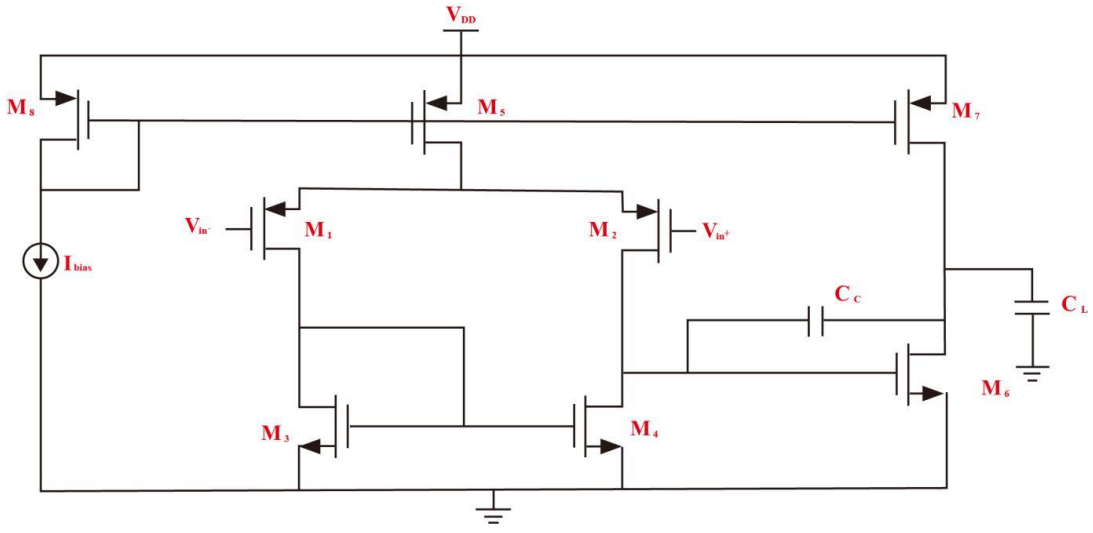

Figure 6: CMOS op amp.

From the GP0 model, the circuit performance and constraint equations in Figure 6 can be derived:

1) The circuit area is shown in formula (4.1):

$$Area = \sum_{i=1}^{8} W_i L_i \tag{4.1}$$

2) The power consumption of the circuit is shown in formula (4.2):

$$P = (V_{DD} - V_{ss})(I_{bias} + I_5 + I_7) \tag{4.2}$$

3) The unity gain bandwidth (UGB) is shown in formula (4.3):

$$UGB = \omega_{c,approx} = \frac{g_{m1}}{C_c} \tag{4.3}$$

4) The slew rate (SR) is shown in formula (4.4):

$$SR = min\left\{\frac{2I_1}{C_c}, \frac{I_7}{(C_c + C_{TL})}\right\} \tag{4.4}$$

After the equation-based and simulation-based optimizations respectively, it is obvious that the advantages and disadvantages of the two methods can be seen, that is, the equation-based optimization is very fast, but the accuracy is low, while simulation-based optimization is very accurate, but slow and takes a lot of time. The authors propose an improved method by combining these two methods.

First of all, although the accuracy of the Pareto optimal solution obtained by equation-based optimization is low, its value is very close to the final optimal solution compared to the random formation of the initial population. Therefore, half of the solutions are extracted from the Pareto optimal solutions obtained from the equation-based optimization, that is, 400 parameter values, which are added to the initial population of NSGA-II. In order to meet the diversity of the population, only half of them are added here, that is, 400 individuals in the initial population of 800 are Pareto optimal solutions based on the optimization of the equation. Another 400 individuals were randomly formed by the program. Then, using the simulation-based optimization design method, the spice simulator is called to evaluate the circuit performance for optimization. After graphical analysis, it is obvious that the improved method has clearly formed the Pareto optimal curve when it evolved to the 80th generation. The proposed model improved the evolutionary efficiency by 40 generations over simulation-based optimized design, equivalent to a time reduction of approximately 8 hours. It only takes about 12 hours to reach the optimization, and the error rate is only 10%. The specific comparison of the three methods is shown in Figure 7:

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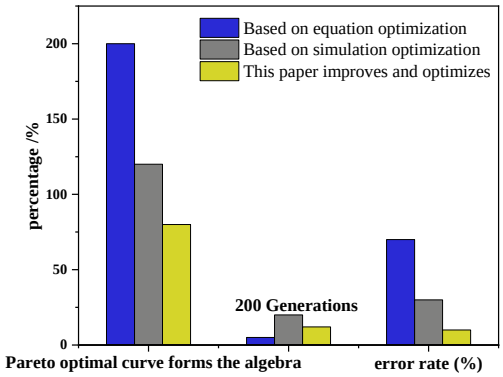

Figure 7: Comparison of three optimization methods.

5 CONCLUSION

On the basis of analyzing and studying the automatic design of analog integrated circuits and multi-objective optimization problems at home and abroad, apply the Pareto multi-objective genetic optimization algorithm to the automated design of analog integrated circuits, evaluate the circuit performance after three different optimization methods and make up for each other, which not only satisfies the high precision of the design, but also greatly improves the design speed and reduces the time consumed. At the same time, the previous synthesis of analog integrated circuit design policy was changed to a single-purpose optimization policy and a multi-purpose optimization policy was introduced such as optimal design, and optimized design. Finally, by completing the optimal design of the CMOS operational amplifier, the Pareto optimal solution set of the operational amplifier is obtained under the condition that the specified performance requirements are met. The primary purpose of this research is to raise the amount of automation in analogue integrated circuit design in order to reduce design time and costs. An improved technique for discovering the Pareto-optimal solution of a CMOS analogue circuit has been devised based on a non-dominant classification evolutionary algorithm. To assess the method's applicability, equation-based, simulation-based, and enhanced methodologies are compared. The optimal design of the op amp is achieved and the time spent is reduced, which fully demonstrates the effectiveness of the method proposed by the author. For the research direction and work, it can be summarized into three points:

1) At present, most circuit optimizations involve circuits with smaller scale and less design changes. The non-dominated sorting genetic algorithm (NSGA-ID) adopted by the author with an elite strategy can better obtain the Pareto optimal solution set, but for large-scale cases, there are many design variables involved. Whether the algorithm can still effectively obtain the optimal solution set, and whether further research and improvement of the algorithm are needed is a direction of future research.
2) The circuit optimization targeted by the author is mainly the optimized design of CMOS operational amplifiers, but for other analog integrated circuits. Such as comparators, filters, oscillator circuits, etc., whether the method proposed in this paper can also be effectively optimized is the direction of future research.
3) Because the solution obtained by multi-objective optimization is a Pareto optimal solution set composed of many Pareto optimal solutions, even if it has converged to the Pareto optimal frontier, the solutions obtained by the next evolution are also many different, so it is difficult to judge the difference between generations. Therefore, generally, the evolutionary algebra is preset as the criterion for algorithm stopping. Obviously, this

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requires subjective judgment. Setting too little evolutionary algebra will not get the global optimal solution, and too much will cause waste of resources, therefore, how to design a clear and effective algorithm stopping criterion remains to be studied.

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